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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,652	07/21/2003	Michael Setton	015290-756	3865

7590 09/09/2004

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EXAMINER

POMPEY, RON EVERETT

ART UNIT	PAPER NUMBER
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2812

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/622,652

Applicant(s)

SETTON, MICHAEL

Examiner

Ron E Pompey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 13 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 22-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 22-40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 22-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinriki et al. (US 5,292,673) and further in view of Gardner et al. (US 6,087,238) and Moslehi (5,322,809).

Shinriki discloses the limitations of:

an interfacial layer (3, fig. 5a), on a silicon semiconductor substrate;

a high dielectric constant layer (2, fig. 5a), that comprises a material that is selected from the group consisting of Ta_2O_5 , $Ta_2(O_{1-x}N_x)_5$, a solid solution of $(Ta_2O_5)_r - (TiO_2)_{1-r}$, a solid solution of $(Ta_2O_5)_s - (Al_2O_3)_{1-s}$, a solid solution of $(Ta_2O_5)_t - (ZrO_2)_{1-t}$, a solid solution of $(Ta_2O_5)_u - (HfO_2)_{1-u}$, on the interfacial layer;

a gate electrode (4, fig. 5a) of an electrically conductive material on the high dielectric constant layer; and

source and drain regions (6, fig. 5d) that are adjacent the gate electrode; and

a pair of spacers (9, fig. 5b) formed adjacent to the gate electrode and formed on the high dielectric constant layer..

(col. 4, Ins. 25-65, col. 5, Ins. 1-68 and col. 6, Ins. 18-21).

3. Shiniriki does not disclose the claimed limitation(s) of:

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a gate electrode having a width of less 0.3-micron covering the high dielectric constant layer;

wherein the insulator layer, with contact wholes, has a substantially planar surface;

a silicide layer on the source and drain regions;

a material that is selected from the group consisting of $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r-(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s-(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t-(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less 1, a solid solution of $(Ta_2O_5)_u-(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate; and

wherein the interfacial layer comprises silicon nitride or silicon oxynitride.

However,

a. Gardner discloses the above claimed limitations regarding:

gate of width less than .3 micron in column(s) 4, line(s) 3-9.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Gardner with Shiniriki, because Gardner discloses what the minimum resolution of photolithography is where Shiniriki is silent on this issue.

b. Moslehi discloses the above claimed limitations regarding:

wherein the interlayer insulator is planar (46, fig. 3a) and silicide (41, fig. 2i) on the source and drain regions.

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Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moslehi with Shiniriki, because Moslehi the silicide on the source and drain provide for a lower resistivity for better electrical conduction for metal contact and the planar insulator keeps topography level so preceding layers can be uniform.


c. Neither Shiniriki, Gardner nor Moslehi disclose the various high dielectric compositions or interfacial layer materials listed above. However, applicant does not disclose these materials to provide unique or different results, when used in a device, from the other materials listed in the group; such as the Ta_2O_5 (high dielectric) or silicon oxide (interfacial layer) disclosed in Shiniriki. Therefore the other materials that are not shown by the prior arts of record do not provide patentable distinction from the materials given in the prior arts of record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E Pompey whose telephone number is (571) 272-1680. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Ron Pompey
AU: 2812
August 7, 2004


RICHARD BOOTH
PRIMARY EXAMINER